

Fig. 1C
PRIOR ART

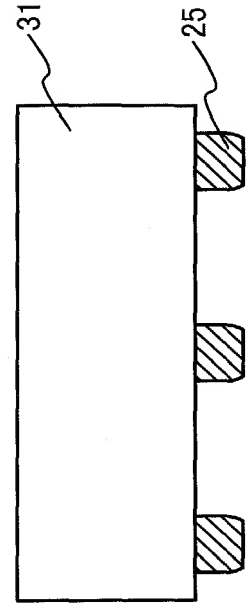


Fig. 1D
PRIOR ART

Fig. 2A

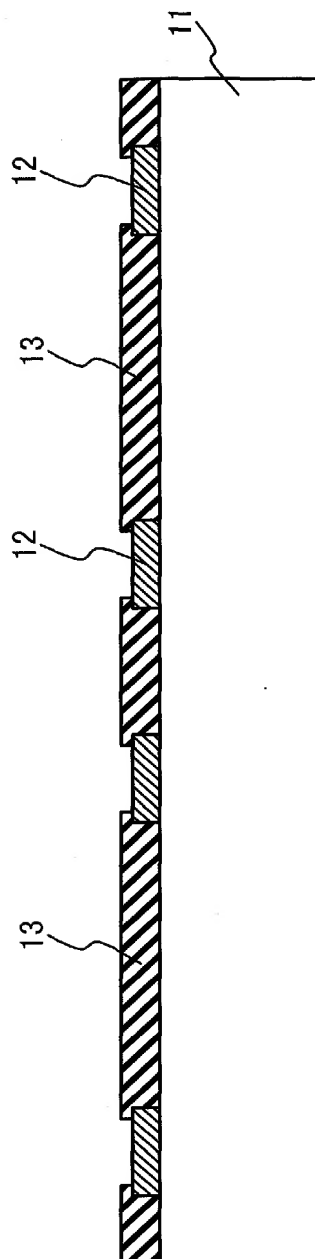


Fig. 2B

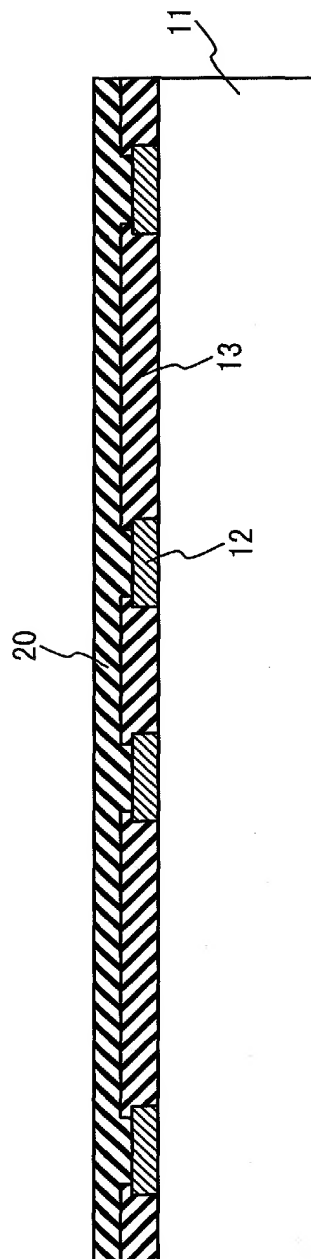


Fig. 2C

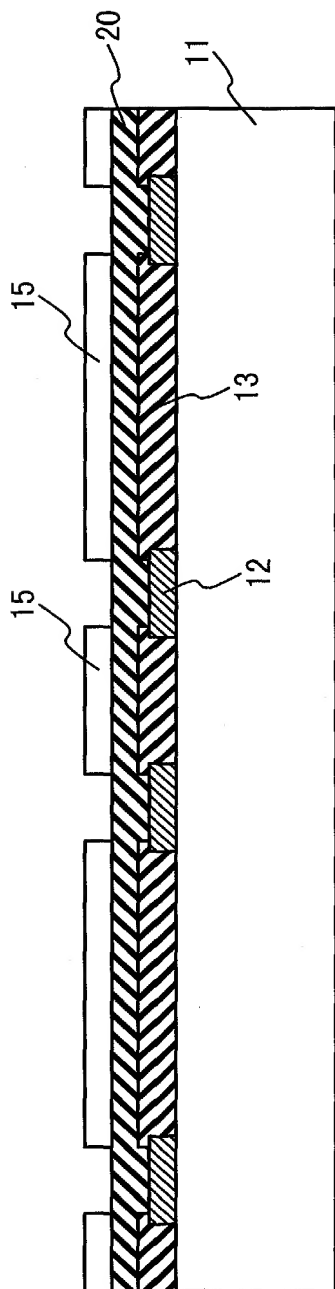
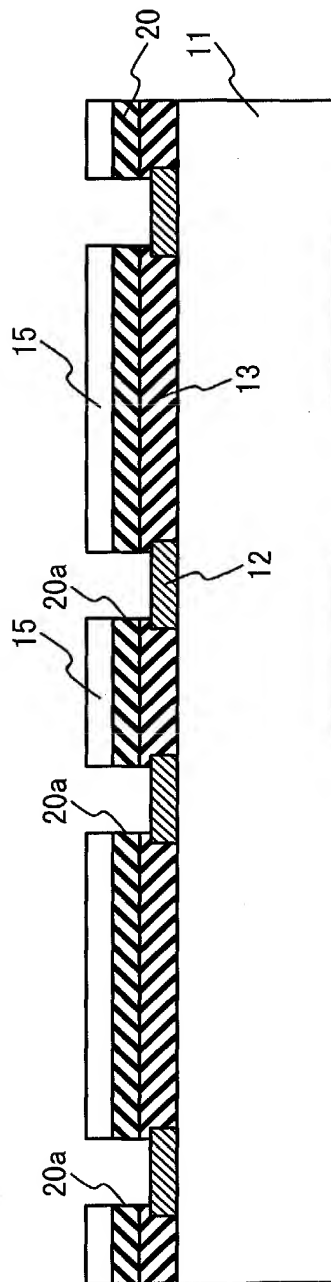
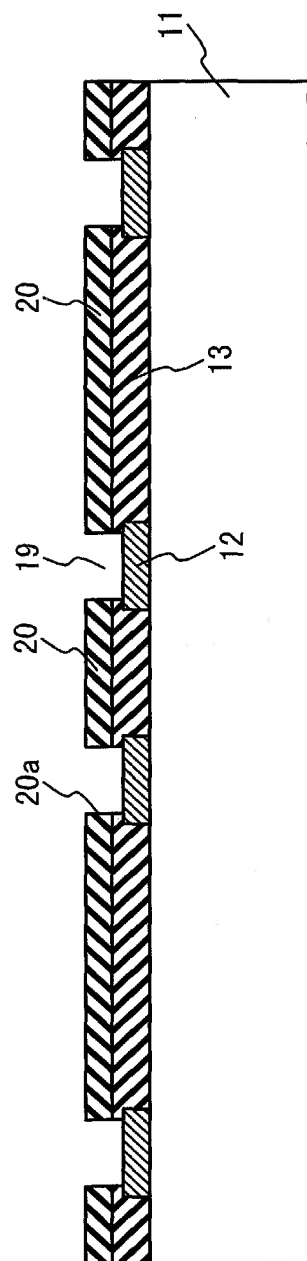


Fig. 2D



File 2E



Fi 8.2F

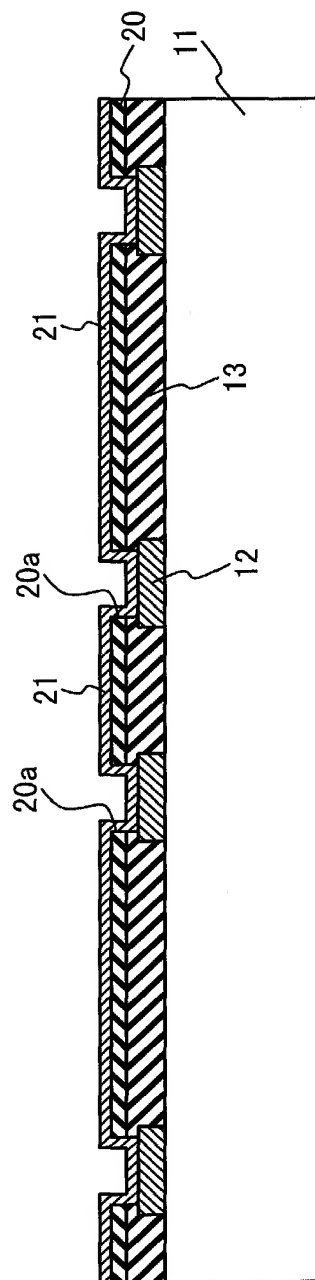


Fig. 2G

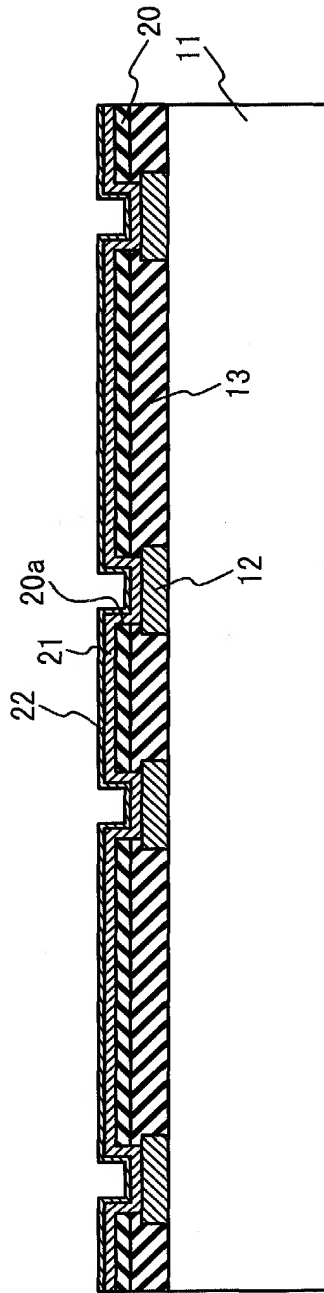
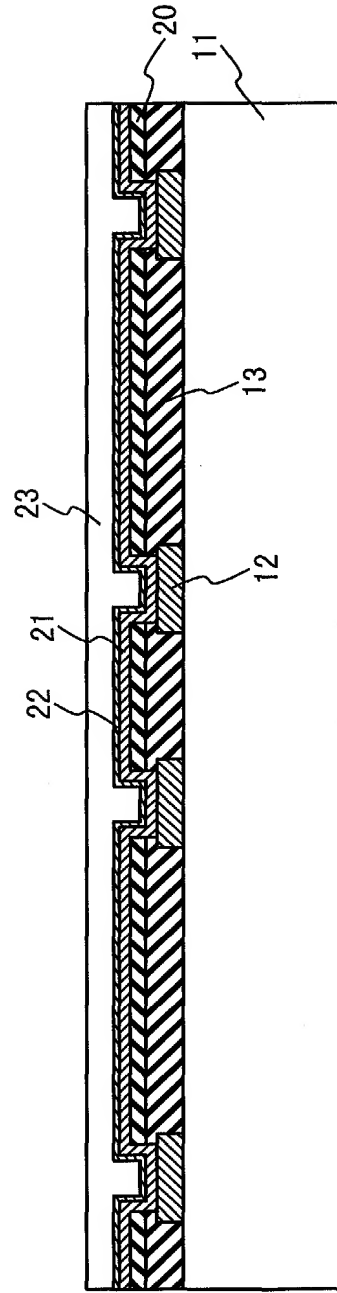


Fig. 2H



11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

Fig. 2I

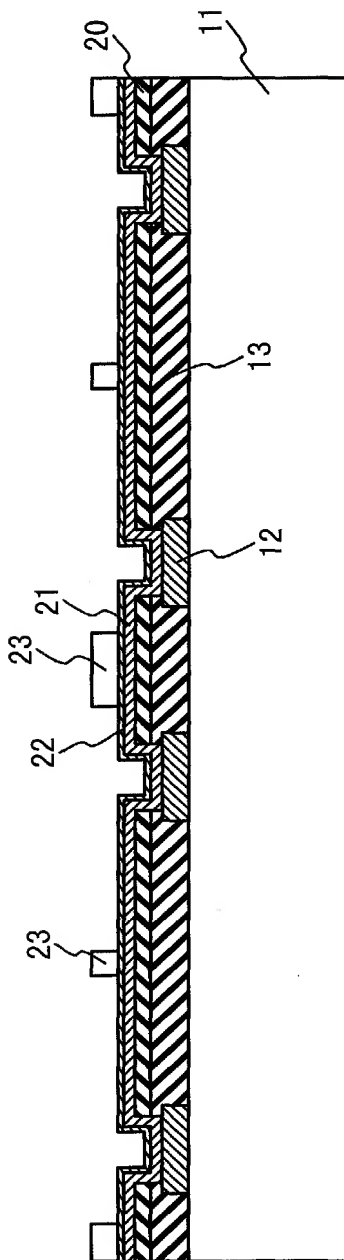


Fig. 2J

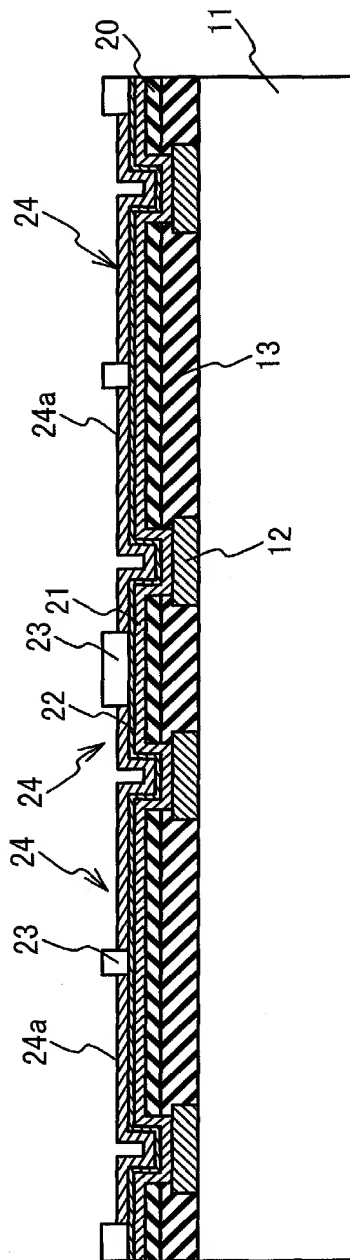


Fig. 2K

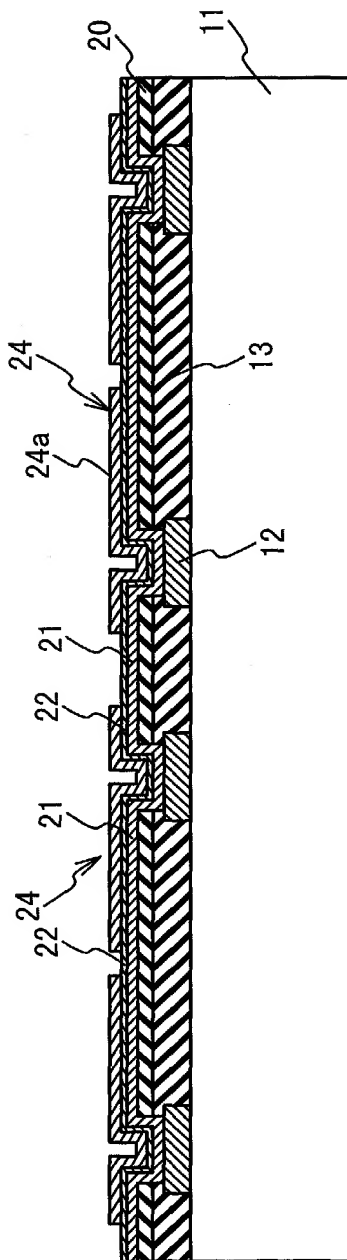


Fig. 2L

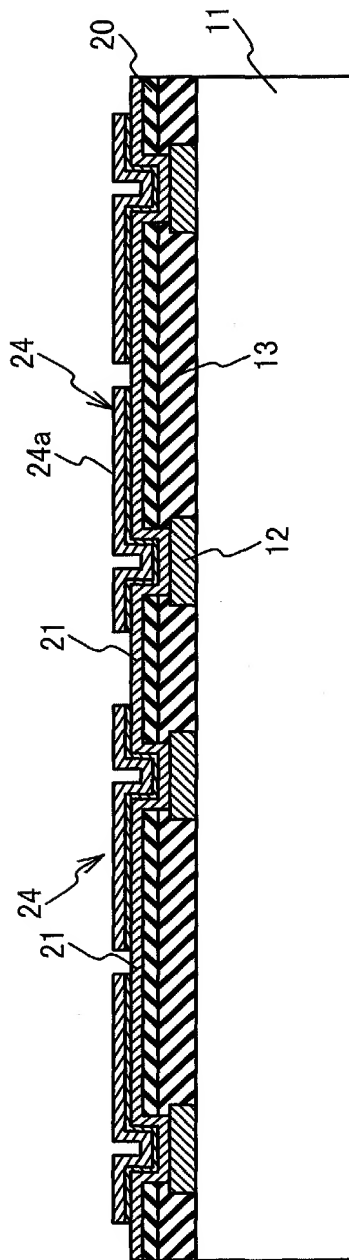


Fig. 2M

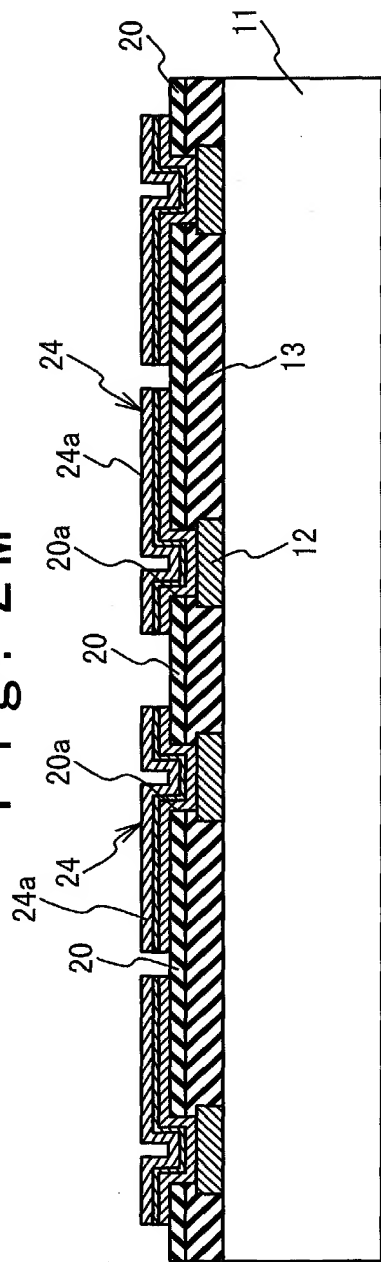
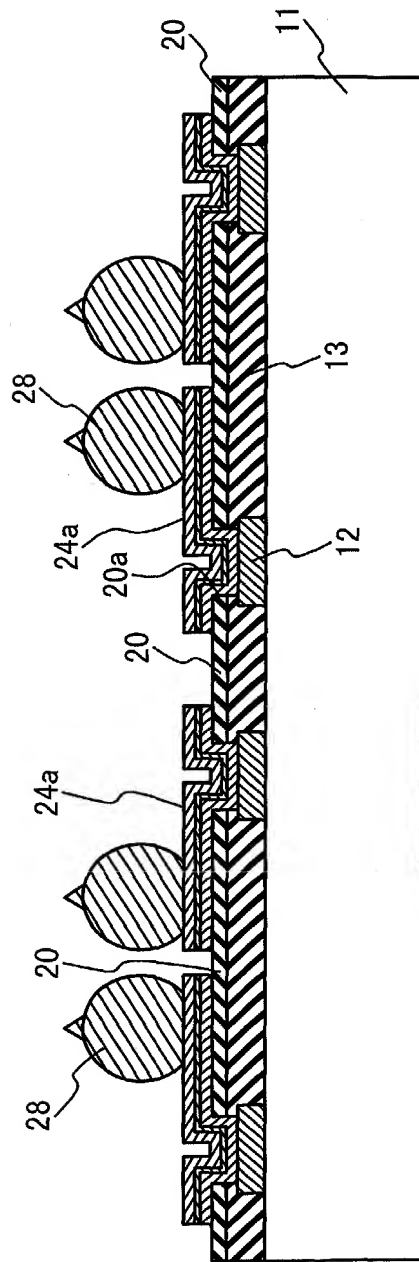


Fig. 2N



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Fig. 20

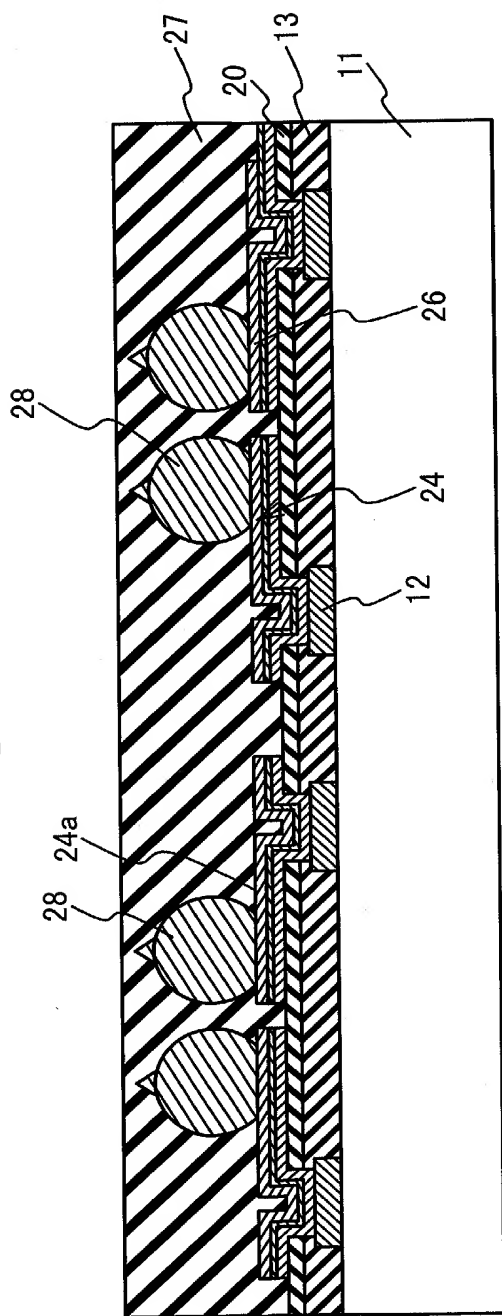
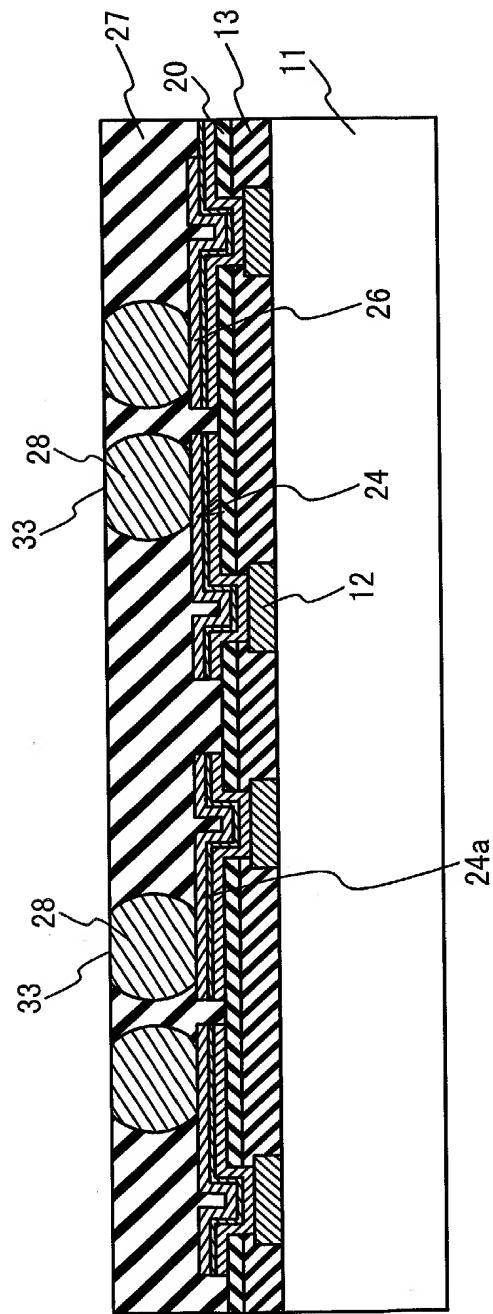


Fig. 2P



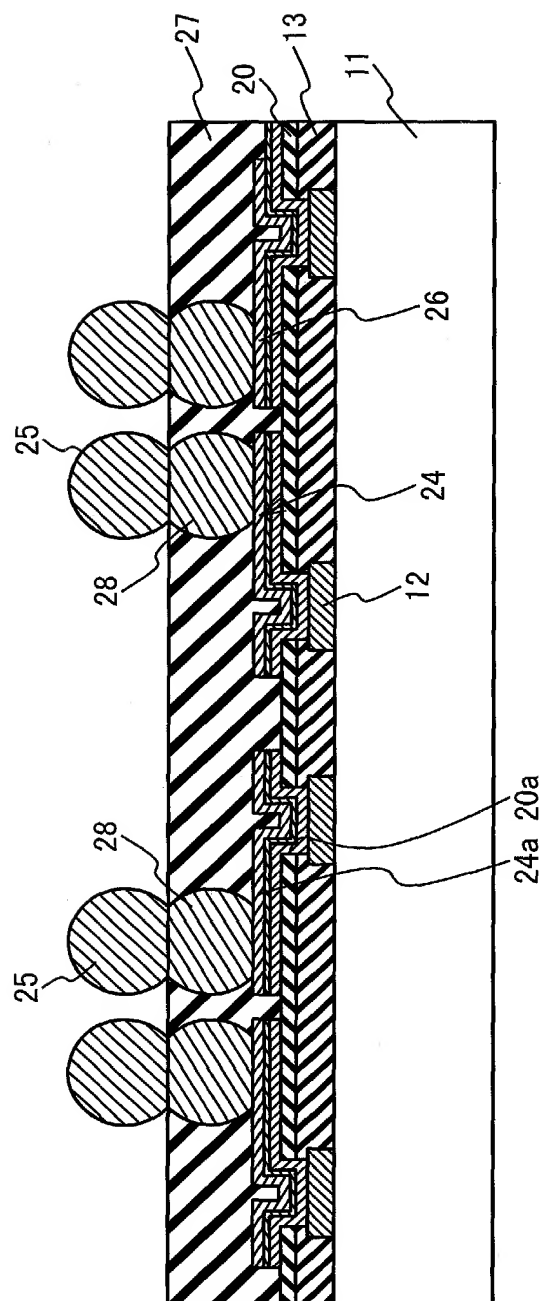
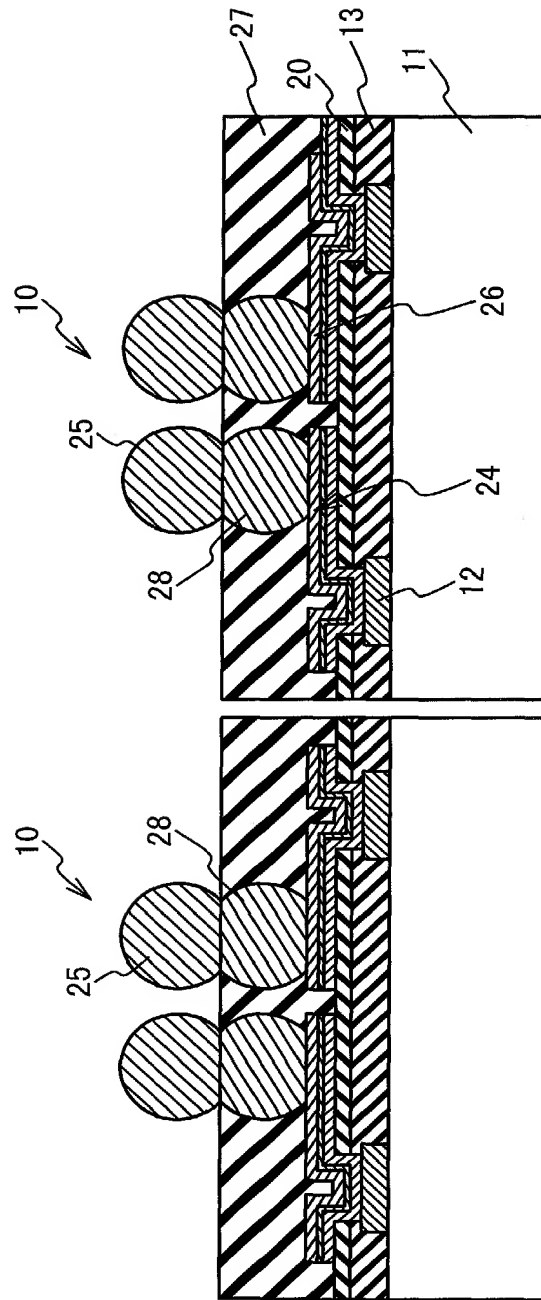
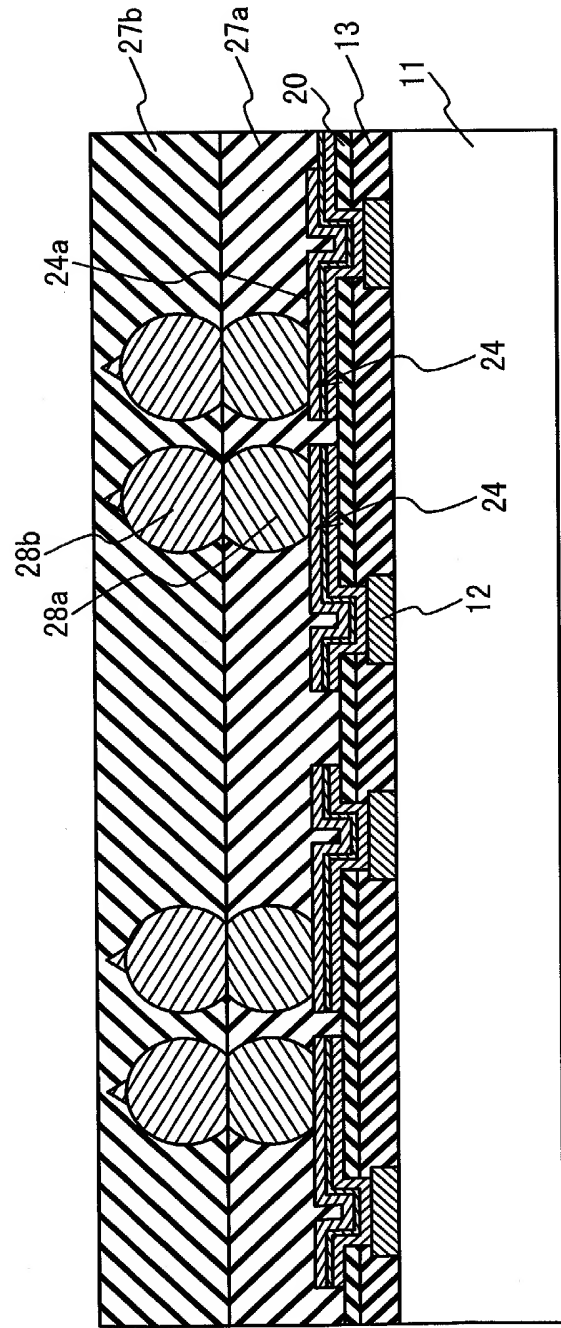
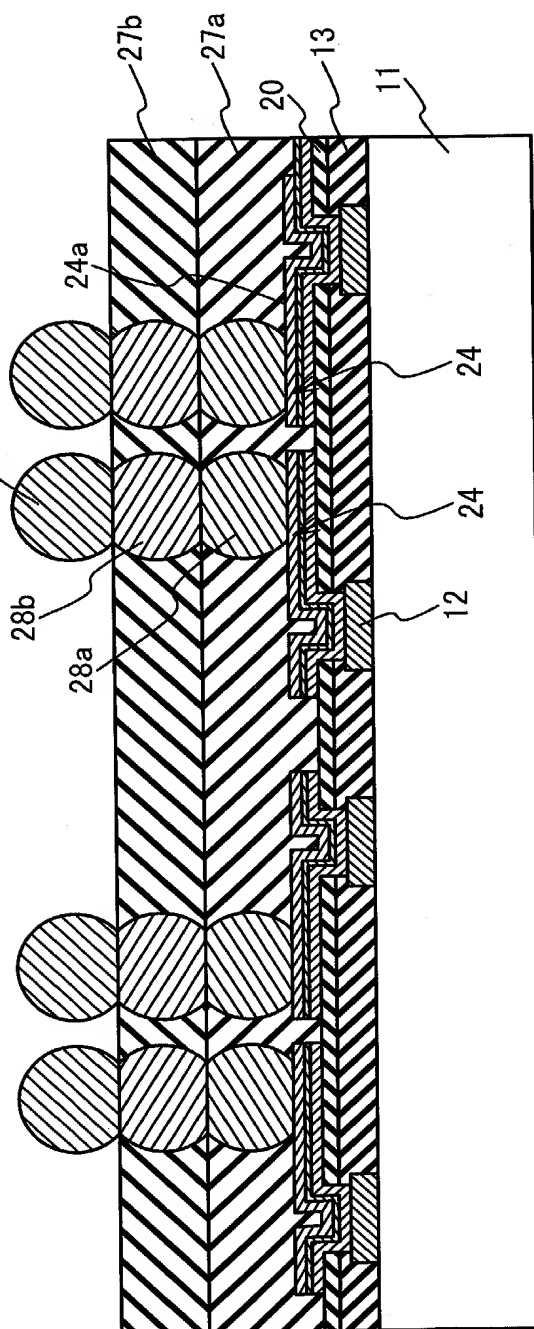
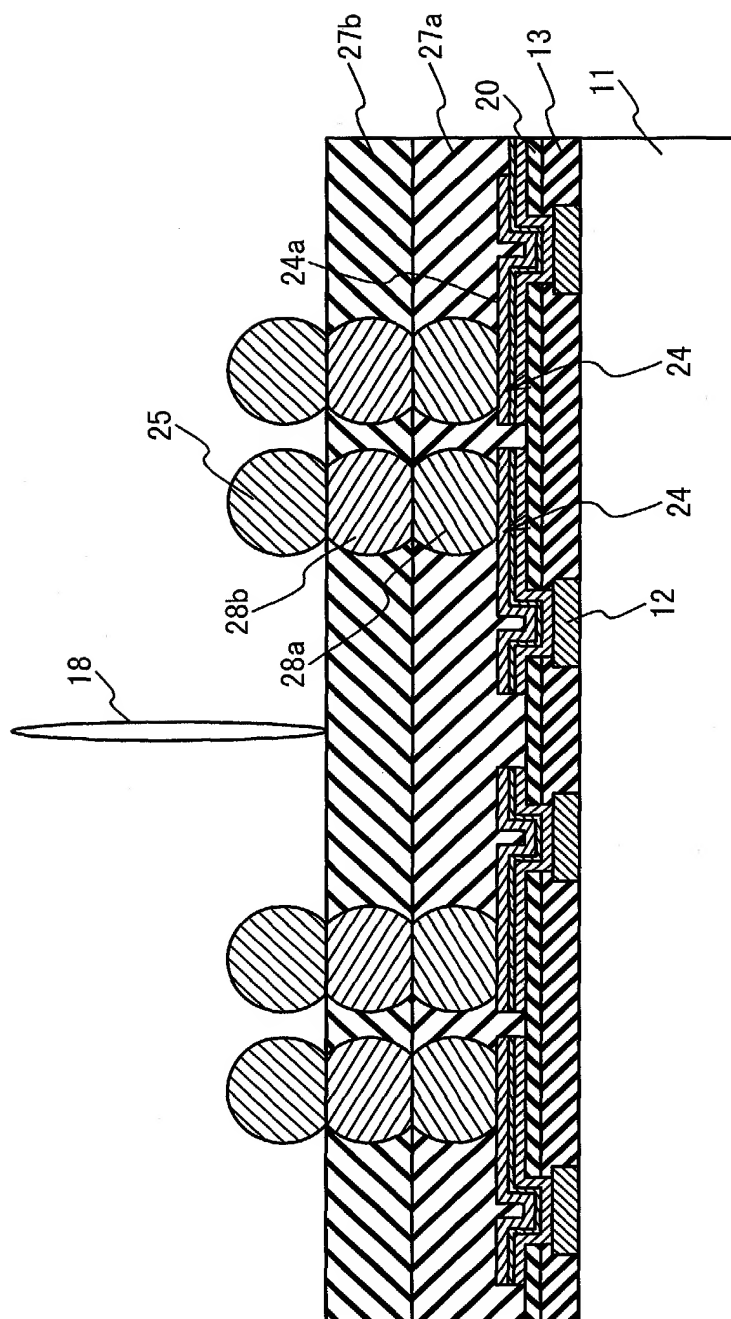


Fig. 2S









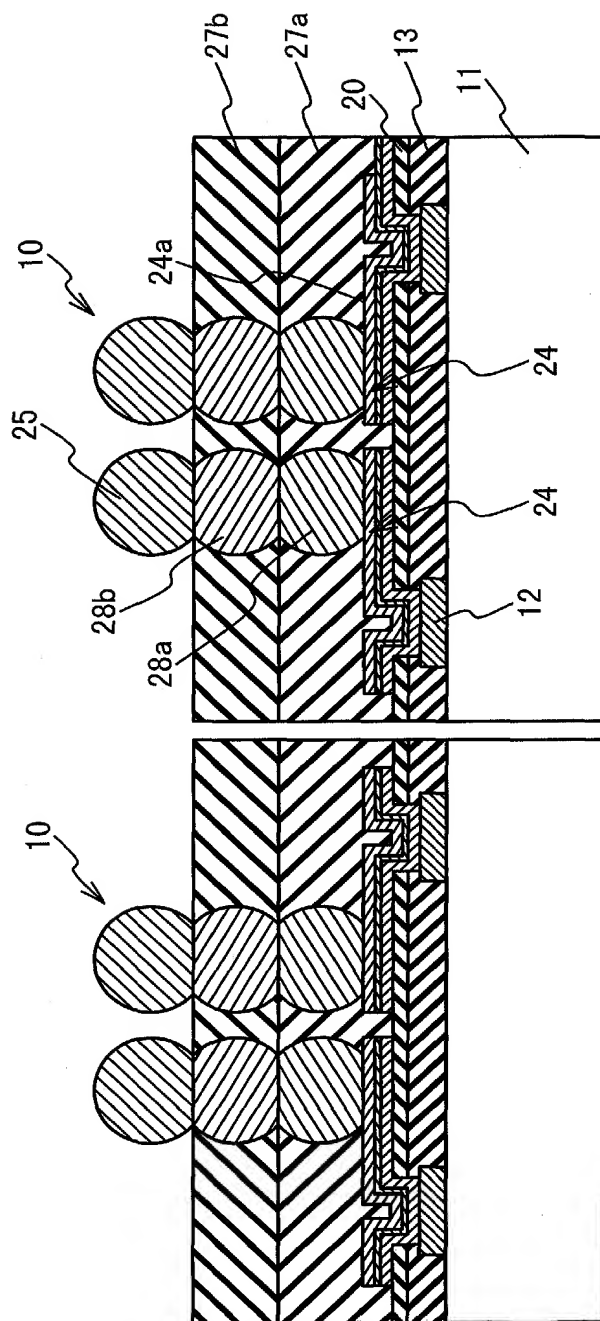


Fig. 4A

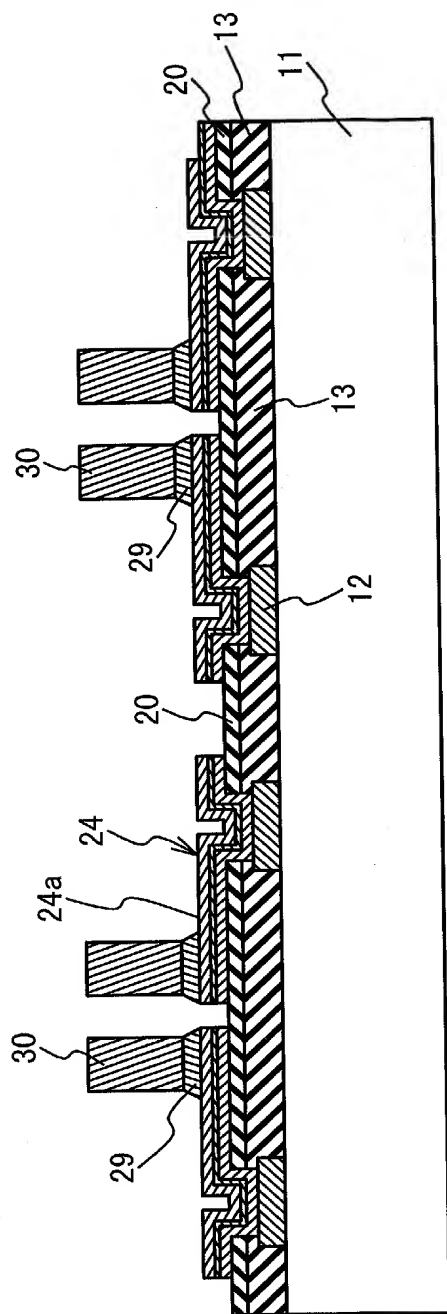


Fig. 4B

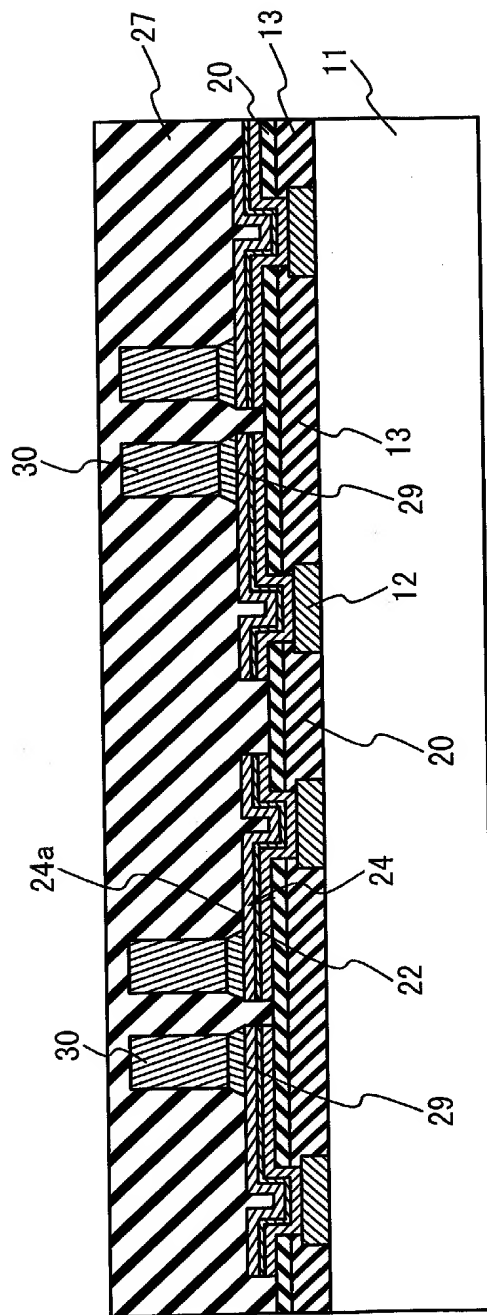


FIG. 4C is a cross-sectional view of a semiconductor device in a first state. The device includes a substrate 11, a gate stack 12, a gate 13, a channel 20, a source 22, and a drain 29. A first conductive layer 30 is formed on the channel 20, and a second conductive layer 34 is formed on the source 22 and drain 29. A first insulating layer 27 is formed on the channel 20, and a second insulating layer 24a is formed on the source 22 and drain 29. The first conductive layer 30 is in contact with the channel 20, and the second conductive layer 34 is in contact with the source 22 and drain 29. The first insulating layer 27 is in contact with the channel 20, and the second insulating layer 24a is in contact with the source 22 and drain 29.

Fig. 4C

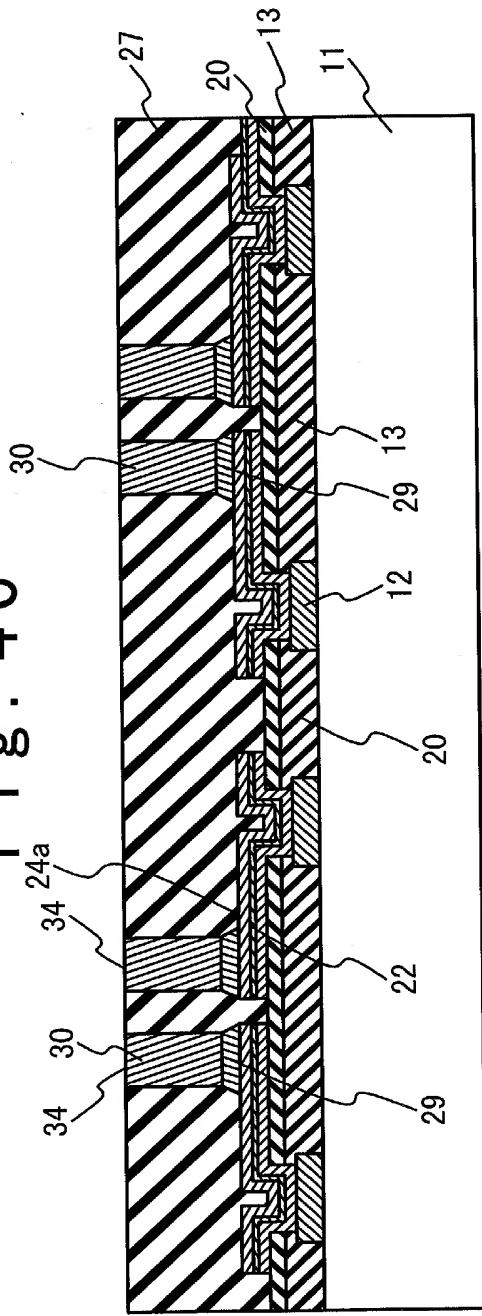
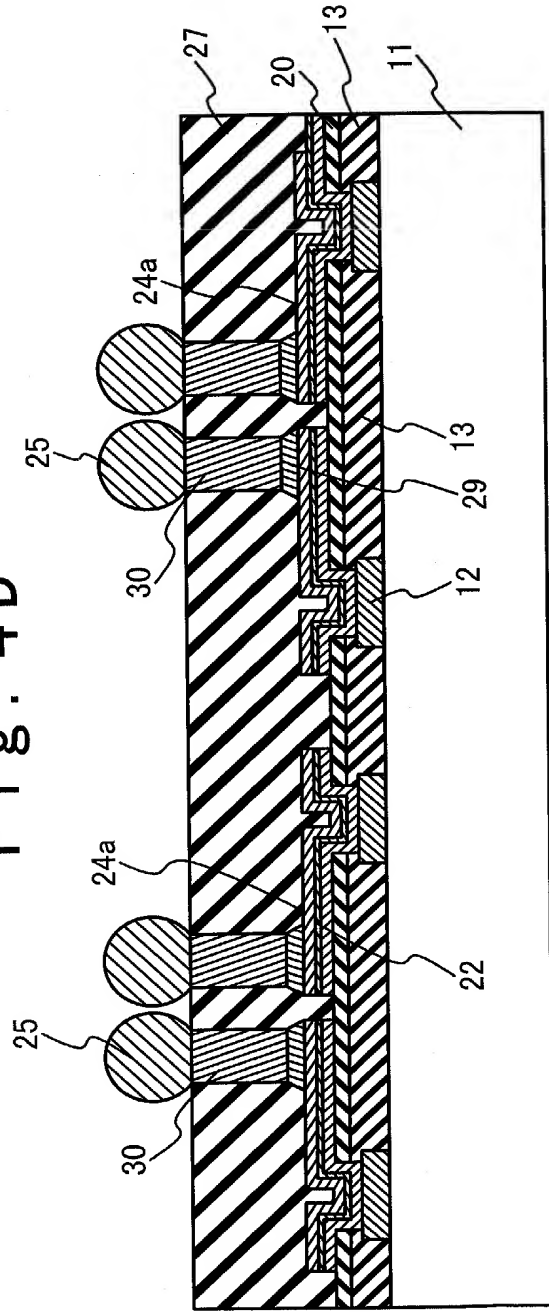


Fig. 4D



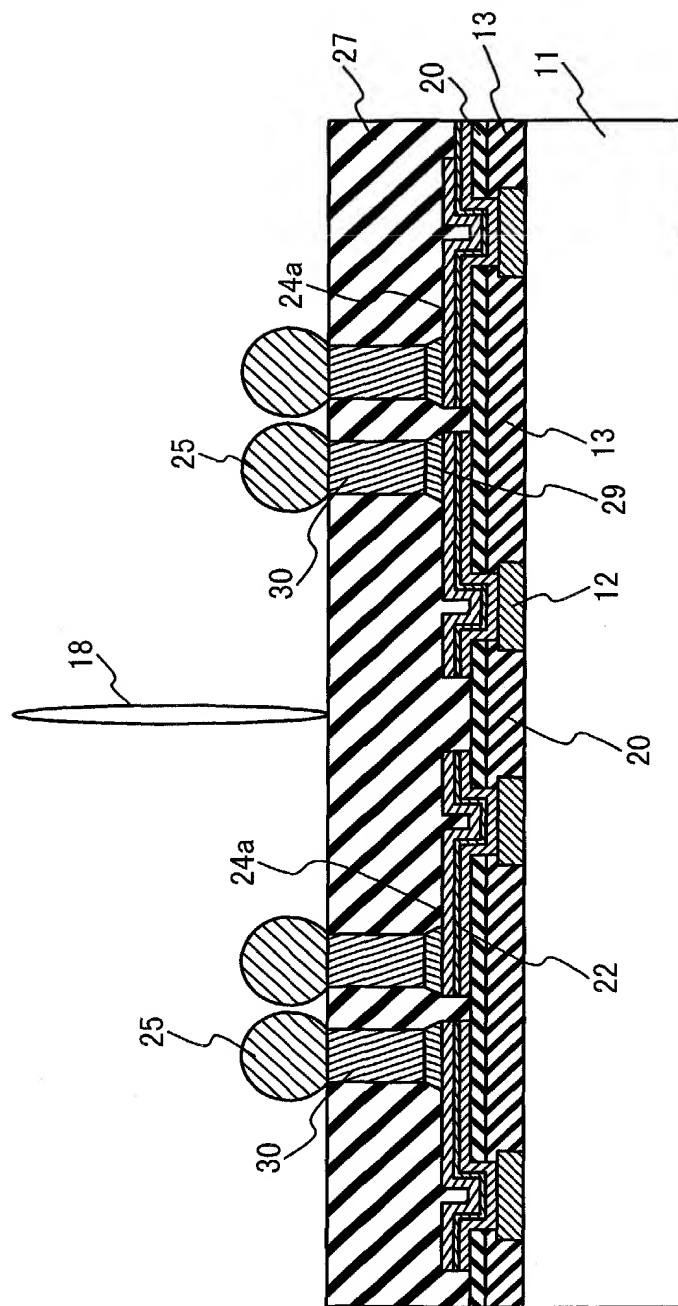


Fig. 4F

